PCT/NZ00/00189

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Intellectual Property Office of New Zealand

REC'D 07 NOV 2000
WIPO PCT

CERTIFICATE

This certificate is issued in support of an application for Patent registration in a country outside New Zealand pursuant to the Patents Act 1953 and the Regulations thereunder.

I hereby certify that annexed is a true copy of the Complete Specification as filed on 29 September 1999 with an application for Letters Patent number 338097 made by TAIT ELECTRONICS LTD.

Dated 5 October 2000.

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH
RULE 17.1(a) OR (b)

Neville Harris
Commissioner of Patents

338097

NEW ZEALAND

PATENTS ACT, 1953

No:

Date:

COMPLETE SPECIFICATION

IMPROVEMENTS RELATING TO EER TRANSMITTERS

We, TAIT ELECTRONICS LIMITED, a New Zealand company, of 558 Wairakei Road, Burnside, Christchurch, New Zealand, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

FIELD OF THE INVENTION

This invention relates to amplification systems for radio frequency signals and in particular but not solely to envelope elimination and restoration (EER) techniques for radio transmitters. These techniques involve primarily digital rather than analog signal processing and a phase-lock-loop (PLL) arrangement having various aspects of phase modulation and phase adjustment. In one embodiment the PLL involves fractional-N frequency division.

BACKGROUND TO THE INVENTION

Mobile communication systems require high frequency power amplifiers for both base station transmitters and portable units carried by users. These amplifiers operate most efficiently at saturation in the non-linear range of their input/output characteristics. Efficiency is important for battery life and weight in the portable units while linearity is important for base stations with multiple carrier transmission. A number of techniques have been developed to compensate for non-linear amplifier operation. Techniques involving modulation feedback from the amplified signal can be divided in two groups depending on how the modulating signal is represented in the baseband. Cartesian amplification systems apply a feedback signal to quadrature components of the modulating signal. Polar loop amplification systems are based on EER techniques with addition of envelope and phase feedback arrangements. The phase feedback forms a PLL although envelope feedback alone may be used.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide for improved amplification systems based on EER techniques. In one form the invention implements largely digital rather than analog processing methods to determine envelope and phase information from a modulating signal and provide feedback from the output signal. In another form the invention implements a PLL with phase modulation by way of a fractional-N divider.

Accordingly in one aspect the invention may broadly be said to consist in an amplification system for a radio transmitter comprising: a processor which determines envelope information and phase information from an input signal, a phase-locked-loop which generates a substantially constant amplitude signal having phase modulation determined by the phase information, and an amplifier which generates an output signal from the constant amplitude signal having amplitude modulation determined by the envelope information.

In another aspect the invention may be said to consist in an amplification system for a radio transmitter comprising: a processor which determines envelope information and phase information from an input signal, and a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information, wherein the phase-locked-loop includes a frequency divider which causes phase modulation of the output signal according to the phase information.

In another aspect the invention may be said to consist in an amplification system for a radio transmitter comprising: a processor which determines envelope information and phase information from an input signal, and a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information, wherein the phase-locked-loop includes an amplifier which modulates the amplitude of the output signal according to the amplitude information.

In still another aspect the invention may be said to consist in an amplification system for a radio transmitter comprising: a processor which determines envelope information and phase information from an input signal, and a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information, wherein the processor modifies the envelope information or the phase information according to feedback from the output signal.

The invention may also broadly be said to consist in any alternative combination of features which are suggested in this specification. All equivalents of these features are included.

BRIEF LIST OF FIGURES

Preferred embodiments of the invention will be described with reference to the drawings of which:

Figure 1 schematically shows a radio transmitter with amplification of a signal by a polar loop feedback system,

Figure 2 shows an amplification system according to the invention,

Figure 3 shows a PLL arrangement for use in the system of Figure 2,

Figure 4 shows an alternative amplification system according to the invention,

Figure 5 shows a PLL arrangement for use in the system of Figure 4,

Figure 6 shows a digital envelope feedback arrangement, and

Figure 7 shows an analog envelope feedback arrangement.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the drawings it will appreciated that the invention may be implemented in various forms and that these embodiments are described by way of example only. Details of existing mobile communication systems will also be known to a skilled reader and need not be given here.

Figure 1 shows EER implemented in a traditional polar loop system. An incoming RF signal I is converted by analog block 10 into polar signals Θ, r respectively containing phase and envelope information. A phase controlled loop including power amplifier 11 operating in saturation then generates an output signal S according to the information for transmission by antenna 12. The phase controlled loop forms a PLL which receives signal Θ and provides a constant amplitude signal to the non-linear amplifier. A power supply to the amplifier receives signal r and thereby controls gain of the amplifier to restore envelope information and produce signal S. The PLL includes a phase comparator or detector 13 which compares the

phases of signal Θ and feedback from signal S to determine the frequency of a voltage controlled oscillator 14. The oscillator in turn provides the constant amplitude signal to the amplifier. Signal r is also modified by addition in block 15 of feedback from signal S. The feedback arrangement includes an optional frequency downconverter 16 followed alternatively for signals Θ, r by an amplitude limiter 16 and envelope detector 17.

Figure 2 shows one embodiment of an amplification system based on EER according to the invention. A digital sub-system or processor arrangement 20, such as a DSP, determines phase and envelope signals P and E from an incoming signal B. A power amplifier 21 generates an output signal S which contains B modulated on a radio frequency carrier. A PLL frequency synthesiser 22 containing a frequency divider such as shown in Figure 3 forms a phase modulation path which feeds the amplifier. An envelope modulation path varies the amplifier gain by way of a modulator 23, which may be a power supply to one stage of the amplifier for example. The digital sub-system also preferably determines a phase offset signal O provided to the PLL over an offset adjustment path as described further below. This provides a fine adjustment of the phase of signal S if required to compensate distortion, and also equalises discrepancies between the phase and envelope modulation paths. A feedback arrangement including detection of envelope and/or phase distortion in signal S preferably provides a feedback signal F for the digital sub-system. A detector and ADC system 24 may be implemented in various ways either separately or incorporated partly in the sub-system. An alternative embodiment in which the amplifier forms part of the PLL is described in Figure 4.

Figure 3 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 2. The arrangement produces an output signal having a frequency which is an integer or fractional multiple of a reference signal and which is modulated according to the phase signal P. A voltage controlled oscillator 30 receives a control signal from phase comparator 31 by way of loop filter 32, and produces a constant amplitude output for the amplifier 21. The loop filter generally integrates an output provided by the comparator according to phase differences between a reference signal from frequency reference 33 and a feedback signal from the controlled oscillator. A phase offset may be introduced between the reference

and feedback signals by signal O from the digital sub-system 20, according to feedback from amplifier 21. This may control the action of an additional current source or sink at the input to the loop filter, for example. A frequency divider 34 under control of a modulator 35 introduces phase signal P from the digital sub-system. The modulator is preferably a sigma-delta arrangement which determines an instantaneous integer value N for the divider in accord with a clock signal from the output of the divider. Signal P forms a digital control word for the modulator.

Figure 4 shows another embodiment of an amplification system based on EER according to the invention. The arrangement is generally similar to that of Figure 2 except that some or all of the stages represented by amplifier 21 and fed by PLL 22 are now included within PLL 40, such as shown in Figure 5. This has an advantage that AM-PM phase errors caused by the amplifier stages are inherently corrected, so that there may be less requirement for a phase adjustment by offset signal O to compensate distortion. The signal may still be required to equalise discrepancies between the phase and envelope modulation paths. Coarse adjustment by a full cycle of the digital sampling period might still be required. On the other hand delay around the loop may be increased with loss of stability and possibly smaller bandwidth. Inclusion of amplification stages introduces additional delay in the loop. The gain and therefore bandwidth must be reduced to maintain stability.

Figure 5 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 4. The arrangement is generally similar to that of Figure 3 except that power amplifier stages 51 being some or all stages of the amplifier 21 in Figure 2, are included in the loop. Envelope information from the digital sub-system 22 is used to modulate the gain of the amplifier stages by way of signal E as before. A limiter 52 is also included to remove the envelope information from signal S before input to the divider 34. The limiter may form part of the input circuitry of the dividers, such as a high gain differential input of the kind found in pre-scalers commonly used in frequency synthesisers.

Figures 6 and 7 show digital and analog systems for obtaining envelope feedback from the power amplifiers 21 or 51 to determine a signal F for the digital sub-system 20. Digital feedback generally requires an envelope detector 60 which may be

implemented in many ways. ADC 61 and DAC 62 are also generally required. Typically the amplitude modulator is a switching type to which the digital signal is directly applied. A combination function 65 of the feedback information with envelope information from the incoming signal B may then be used to form signal E for modulation of the amplifier. Analog feedback also requires an envelope detector 70. A combination function 75 of the feedback with the envelope information takes place outside the digital sub-system before formation of signal E.

Further feedback of distortion information may be provided by one or more signals F as shown in Figures 2 and 4, in addition to or instead of phase or envelope feedback. This would enable pre-distortion of the envelope and phase information signals E and P. Processing to determine channel power or bandwidth effects might be used in signal S, for example.

CLAIMS:

1. An amplification system for a radio transmitter comprising:

a processor which determines envelope information and phase information from an input signal,

a phase-locked-loop which generates a substantially constant amplitude signal having phase modulation determined by the phase information, and

an amplifier which generates an output signal from the constant amplitude signal having amplitude modulation determined by the envelope information.

2. A system according to claim 1 wherein:

the phase-locked-loop includes a frequency divider which is modulated according to the phase information.

3. A system according to claim 2 wherein:

the frequency divider is modulated by a sigma-delta modulator which is controlled by the processor.

4. A system according to claim 1 wherein:

the phase-locked-loop includes a phase comparator in which a phase offset between a reference signal and a feedback signal is adjusted by the processor.

5. A system according to claim 4 wherein:

the processor adjusts the phase offset of the comparator according to feedback from the output signal from the amplifier.

6. A system according to claim 1 wherein:

the processor modifies the envelope information according to feedback from the output signal from the amplifier.

7. A system according to claim 1 wherein:

the processor modifies the phase information according to feedback from the output signal from the amplifier.

8. An amplification system for a radio transmitter comprising:

a processor which determines envelope information and phase information from an input signal, and

a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information,

wherein the phase-locked-loop includes a frequency divider which causes phase modulation of the output signal according to the phase information.

9. A system according to claim 8 wherein:

the phase-locked-loop includes an amplifier which causes amplitude modulation of the output signal according to the envelope information.

10. A system according to claim 8 wherein:

the frequency divider includes a digital modulator which operates in response to a control word received from the processor.

11. A system according to claim 8 wherein:

the processor predistorts the phase modulation of the output signal according to the envelope information and feedback from the output signal.

12. A system according to claim 11 wherein:

the processor predistorts the phase modulation of the output signal by modifying the phase information.

13. A system according to claim 11 wherein:

the processor predistorts the phase modulation of the output signal by modifying the phase offset of a phase comparator in the phase-locked-loop.

14. A amplification system for a radio transmitter comprising:

a processor which determines envelope information and phase information from an input signal, and

a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information,

wherein the phase-locked-loop includes an amplifier which modulates the amplitude of the output signal according to the amplitude information.

15. An amplification system for a radio transmitter comprising:

a processor which determines envelope information and phase information from an input signal, and

a phase-locked-loop controlled by the processor which generates a radio frequency output signal containing the envelope information and the phase information,

wherein the processor modifies the envelope information or the phase information according to feedback from the output signal.

16. An amplification system substantially as herein described with reference to the accompanying drawings.

17. Each invention herein.

Tait Electronics Limited
By the authorised agents
A. J PARK & SON
Per

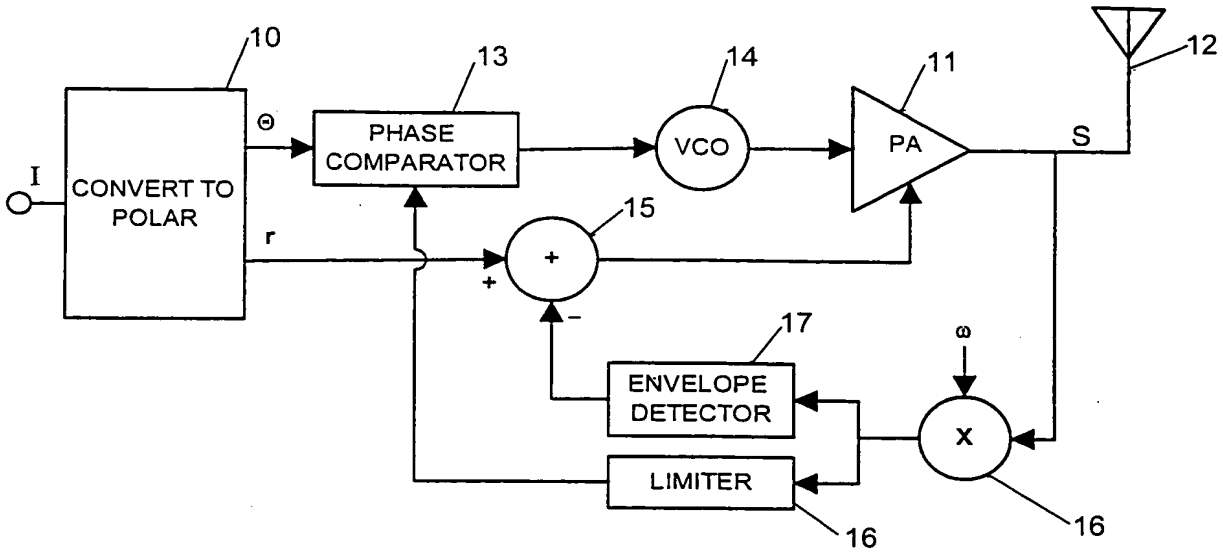


FIG. 1

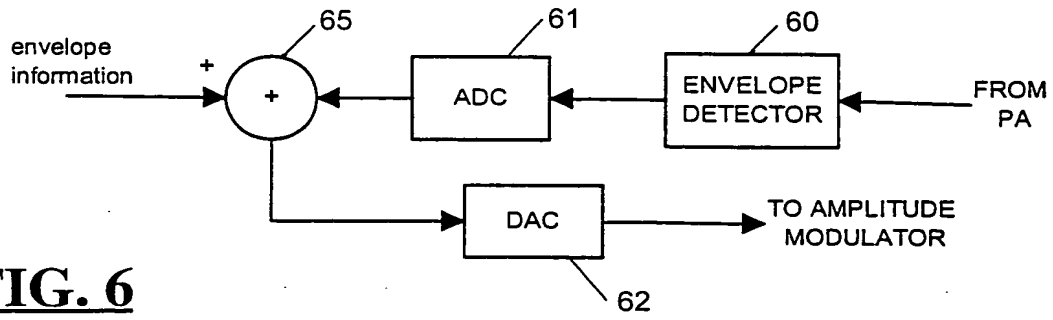


FIG. 6

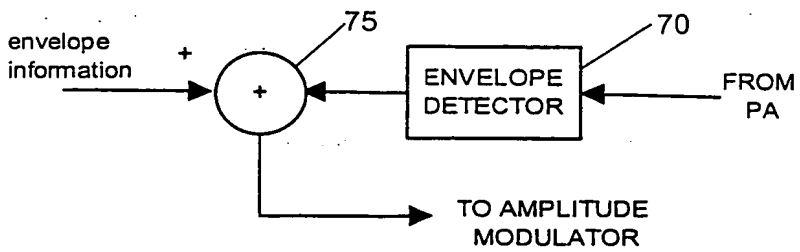
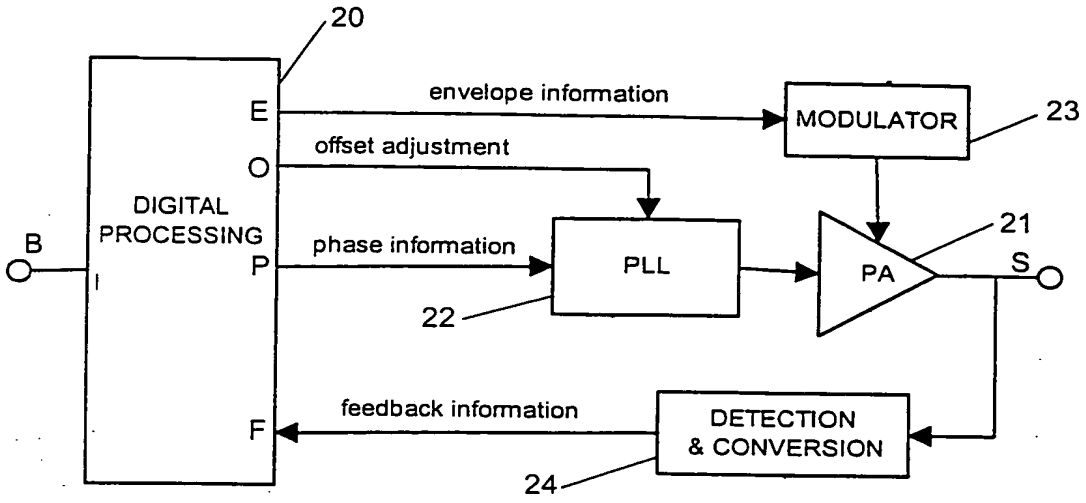


FIG. 7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PLL
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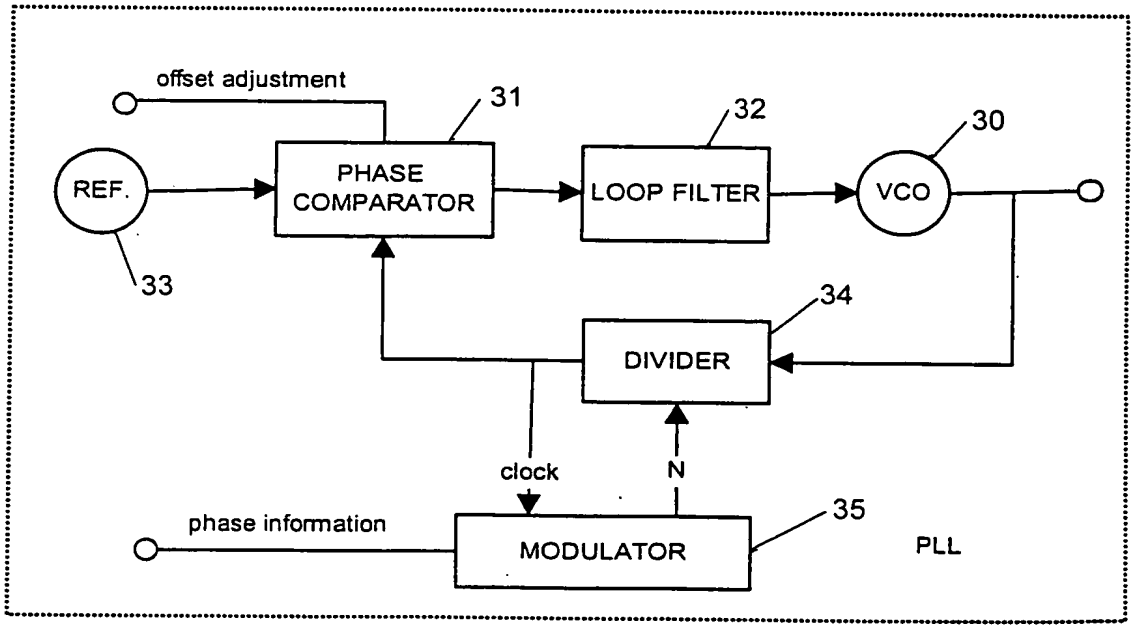
feedback information
F
DETECTION
& CONVERSION
24

FIG. 2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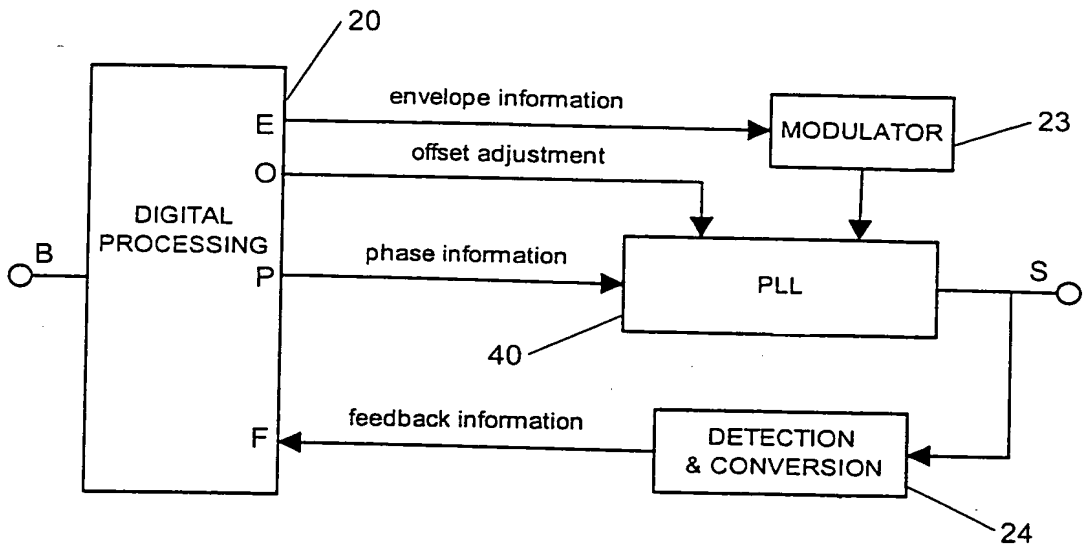
PLL

FIG. 3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& CONVERSION
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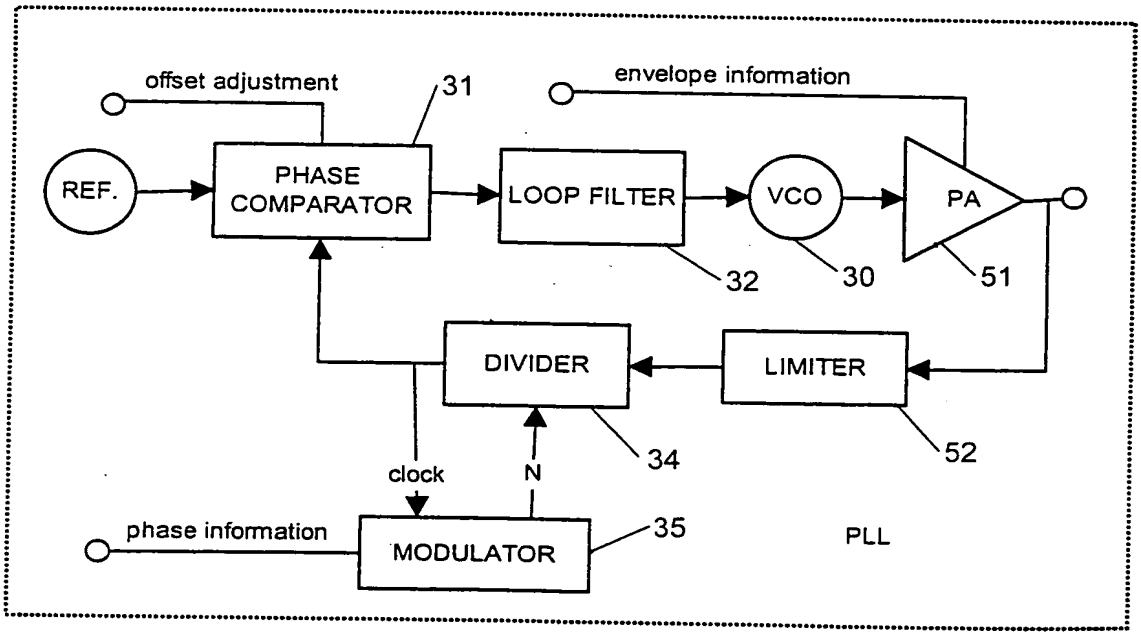
FIG. 4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LIMITER
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clock
N
phase information
MODULATOR
35
PLL

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NZ00/00189

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H03C 5/00, H04L 27/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC GLOBAL

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 99/54994 A (ROCKWELLSEMICONDUCTOR SYSTEMS, INC.) 28 October 1999 The whole document	1-10
X	EP 360178 A (HUGHES NETWORK SYSTEMS, INC.) 28 March 1990 The whole document	1,2
A	WO 99/05783 A (MOTOROLA, INC.) 4February 1999 The whole document	1-10

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
4 January 2001

Date of mailing of the international search report
11 January 2001

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NZ00/00189

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5705959 A (O'LOUGHLIN) 6 January 1998 The whole document	1-10

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/NZ00/00189

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	9954994	US	5966051				
EP	360178	AU	41633/89	CA	1320604	JP	2180453
		US	4972440				
WO	9905783	CN	1234922	DE	19881110	FI	990600
		FR	2766637	GB	2331881	SE	9901094
		US	5886572				
US	5705959	NONE					

END OF ANNEX